IN THE SPECIFICATION:

The paragraph at page 24, line 6 – page 25, line 7, is replaced with the following paragraph:

Steps 514 through 522 will now be applied to the array of FIG. 4. For the x axis, which is to be considered first according to the convention adopted above, the initial processor (which is also the source processor 470) is at location (2,2), the target processor is at location (5,2), and *N* is equal to 6. Therefore, the result (of directly sending the packet from the initial processor to the target processor) for the x axis is exactly equal to *N*/2 moves (5 minus 2)). This situation corresponds to step 522 and, thus, the packet is to be randomly sent either directly or indirectly (by the method randomly returning to step 518 or step 520, respectively). For the purpose of illustration, a description of directly sending the packet from the initial processor to the target processor (i.e., step 518) in the x axis will be given. Prior to directly sending the packet, a 0-bit is added to the packet (since the packet is to be sent directly and, thus, is to be injected in the positive x direction), and the packet is placed in the first queue. As shown by the dotted lines in Fig. 4, the packet is then sent directly as follows: (2,2)->(3,2)->(4,2)->(5,2). It is to be noted that since the packet is being inserted into the positive x direction (by positive x direction logic), it can only be removed at the target processor when arriving in the same direction (positive x).

The paragraph at page 25, line 8 – page 26, line 5, is replaced with the following paragraph:

Next, for the y axis, the initial processor (previously the target processor for the x axis) is at location (5,2), the target processor (which is also the destination processor

480) is at location (5,7), and N is equal to 8. Thus, the result (of directly sending the packet from the initial processor to the target processor) for the y axis is greater than $N/2$ moves (7 minus 2). This situation corresponds to step 520 and, thus, the packet is to be indirectly sent (from the initial to the target processor) so as to wrap around each end processor. Prior to indirectly sending the packet, a 1-bit is added to the packet (since the packet is to be sent indirectly and, thus, is to be injected in the negative y direction), and the packet is placed in the second queue. As shown by the dotted lines in Fig. 4, the packet is then sent indirectly as follows: (5,2)->(5,1)->wrap (bottom output 456 to bottom input 457, of bottom end processor 455)->(5,2)->(5,3)->(5,4)->(5,5)->(5,6)->(5,7)->(5,8)->wrap (right output 466 to right input 467, of processor 465)->(5,7). Note that the packet was ignored the first time it passed the target node. The target node receives the packet on the second pass of the packet.